**FSM OF BCD COUNTER**

# LAB # 06



# Spring 2021

[**CSE-308L Digital System Design Lab**](https://classroom.google.com/u/0/c/MzA5OTAyNzE2MzM2)

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Class Section: **B**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

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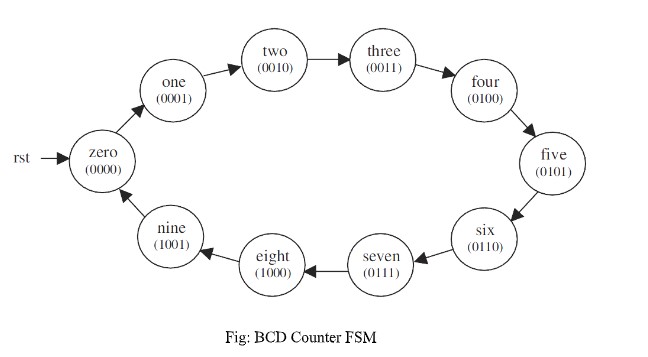
**OBJECTIVES:**

This lab will enable students to:

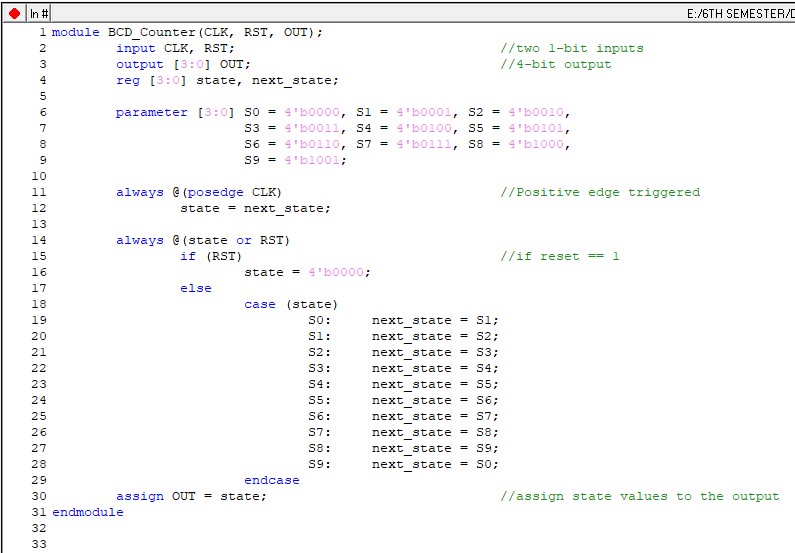
* Code using Behavioral level modeling
* Implement FSM of BCD Counter

**TASK:**

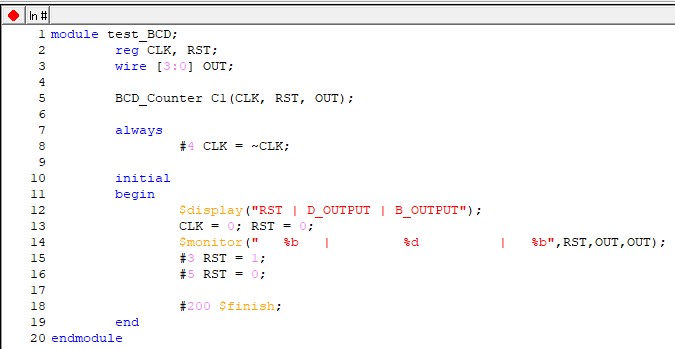
Develop a Verilog model for the FSM of BCD Counter (0 – 9), which rolls over when it reaches 9 to 0.



**CODE:**

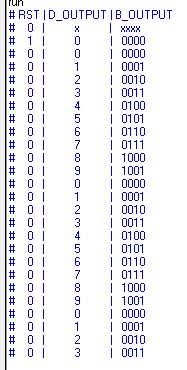


**TestBench:**

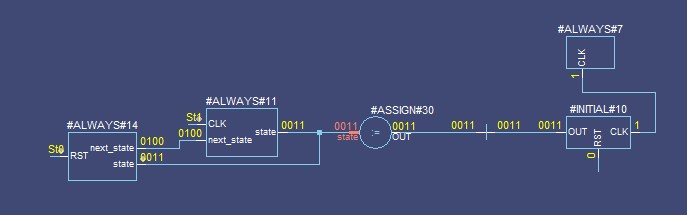


**OUTPUTS**

**Truth Table:**



**Data Flow:**



**Wave Form:**

